a plurality of [floating lateral clamp] diodes connected to the pad so that a first [floating lateral clamp] diode is connected to the pad and the positive line, and a second [floating lateral clamp] diode is connected to the pad and the negative line, a [floating lateral clamp] diode of the plurality of [floating lateral clamp] diodes having:

a well of a second conductivity type formed in the substrate, the well having a top surface and a dopant concentration;

a plurality of spaced-apart first regions of the first conductivity type formed in the well, each first region having a top surface, the plurality of first regions being electrically connected together, and formed in the well so that the top surface of the well encircles the top surface of each first region; and

a second region of the second conductivity type formed in the well, the second region having a top surface, and being formed so that the top surface of the second region encircles the top surface of the well that encircles the top surface of each first region, the second region having a dopant concentration that is greater than the dopant concentration of the well.

10. (Twice Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a pad;

an electrostatic discharge (ESD) positive line, the ESD positive line not being connected to a voltage source;

an ESD negative line; and

a plurality of [floating lateral clamp] diodes connected to the pad so that a first [floating lateral clamp] diode is connected to the pad and the positive line, and a second [floating lateral clamp] diode is connected to the pad and the negative line, a [floating lateral clamp] diode having:

a well of a second conductivity type formed in the substrate, the well having a surface and a dopant concentration; [and]

a first region of the second conductivity type formed in the well, the first region having a surface, and a dopant concentration that is greater than the dopant concentration of the well; and

a plurality of spaced-apart second regions of the first conductivity type, each second region having a surface, the plurality of second regions being electrically connected together, and formed in the first region so that the surface of the first region encircles the surface of each second region.

15. (Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring;

a plurality of ESD positive lines, the plurality of positive lines not being connected to a steady voltage source;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each positive line is connected to the negative ring via an ESD switch;

a plurality of first [floating lateral clamp] diodes connected to the pads so that each first

[floating lateral clamp] diode is connected to a pad and the negative ring; and

a plurality of second [floating lateral clamp] diodes connected to the pads so that each second [floating lateral clamp] diode is connected to a pad and a positive line.

17. (Amended) The chip of claim 15 wherein a first [floating lateral clamp] diode comprises:

a well of a second conductivity type formed in the substrate, the well having a surface and a dopant concentration; and

a plurality of spaced-apart first regions of the first conductivity type, each first region having a surface, the plurality of first regions being electrically connected together, and formed in the well so that the surface of the well encircles the surface of each first region.

20. (Amended) The chip of claim 15 wherein a first [floating lateral clamp] diode comprises:

a well of a second conductivity type formed in the substrate, the well having a surface and a dopant concentration; and

a first region of the second conductivity type formed in the well, the first region having a surface, and a dopant concentration that is greater than the dopant concentration of the well;

a plurality of spaced-apart second regions of the first conductivity type, each second region having a surface, the plurality of second regions being electrically connected together, and formed in the first region so that the surface of the first region encircles the surface of each second region.

34. (Amended) The chip of claim [32] 33 wherein the ESD switches are [located between two adjacent corners of the chip] uniformly spaced apart around the periphery of the chip.

35. (Amended) The chip of claim 34 wherein [an ESD switch is positioned adjacent to one of the two adjacent corners] the number of ESD switches is even.

Please add the following new claim 37:

--37. The chip of claim 1 wherein the first diode is formed below the positive line and the second diode is formed below the negative line.--

REMARKS

This is an amendment under 37 CFR §1.116. The purpose of this amendment is to put the claims in condition for allowance or, alternately, in better form for appeal. The amendments and specific arguments herein, to the extent they were not presented earlier, are now presented because they are necessitated by the reference citations and arguments made by the Examiner in the last office action. It is submitted that these amendments do not raise new issues and do not require any further searching.

Since this response is being filed within two months of the mailing date of the final rejection, the courtesy of an advisory action is respectfully requested.

Claims 1, 5-6, 10-11, 17-23, and 32-37 are now in this application. Claims 1, 10, 15, 17, 20, and 34-35 have been amended. Claims 1, 10, 15, 17, and